

CLAIMS

We claim:

1 1. A semiconductor structure, comprising:
2 a first substrate;
3 a second substrate joined to the first substrate;
4 a plurality of contacts between the first substrate and
5 the second substrate; and
6 a plurality of first solder bumps connected between the
7 first substrate and the second substrate for aligning the
contacts.

1 2. The semiconductor structure according to claim 1,
2 wherein the contacts have a different composition than the
first solder bumps.

1 3. The semiconductor structure according to claim 1,
2 wherein at least one of the first substrate and the second
substrate is an integrated circuit chip.

1 4. The semiconductor structure according to claim 1,
wherein the contacts comprise second solder bumps.

wherein the contacts each have a diameter of about 10 μm .

1 12. The semiconductor structure according to claim 1,
2 wherein the contacts each have a diameter of less than about
10 μm .

1 13. The semiconductor structure according to claim 1,
wherein the contacts have a pitch of less than about 100 μm .

1 14. The semiconductor structure according to claim 1,
wherein the contacts have a pitch of about 30 μm .

1 15. The semiconductor structure according to claim 1,
2 wherein the contacts have a diameter about 20% of the
diameter of the first solder bumps.

1 16. The semiconductor structure according to claim 1,
2 wherein the contacts comprise a material having a higher
melting point than the first solder bumps.

1 17. The semiconductor structure according to claim 1,
2 wherein an upper surface of the contacts and an upper
surface of the first solder bumps are co-planar.

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1 24. The semiconductor structure according to claim 1,
2 wherein the contacts comprise an optical transmitter and an
optical receiver.

1 25. The semiconductor structure according to claim 1,
2 wherein at least one of the first substrate and the second
3 substrate is an integrated circuit chip, and the contacts
4 are sufficiently small to permit alignment of individual
devices on the integrated circuit chips.

1 26. A method of fabricating a semiconductor structure,
2 the method comprising:

- 3 providing a first substrate and a second substrate;
- 4 providing contacts on one of the first substrate and
- 5 the second substrate;
- 6 providing first solder bumps on one of the first
- 7 substrate and the second substrate;
- 8 mounting the first substrate on the second substrate;
- 9 and

10 reflowing the first solder bumps for surface tension
aligning of the contacts.

1 27. The method according to claim 26, wherein the
2 contacts have a different composition than the first solder

bumps.

1 28. The method according to claim 26, wherein at least
2 one of the first substrate and the second substrate is an
integrated circuit chip.

1 29. The method according to claim 26, wherein the
contacts comprise second solder bumps.

1 30. The method according to claim 29, further
2 comprising:

3 reflowing the second solder bumps, wherein the second
4 solder bumps ball up to make contact between the first
substrate and the second substrate.

1 31. The method according to claim 29, wherein the
2 second solder bumps comprise a material having a higher
3 melting point than the first solder bumps, and reflowing the
4 second solder bumps requires heating the second solder bumps
5 to a higher temperature than reflowing the first solder
bumps.

1 32. The method according to claim 29, wherein the
2 second solder bumps are provided with a smaller size than

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1 39. The method according to claim 26, wherein the
2 contacts each are provided with a diameter of less than
about 50 μm .

1 40. The method according to claim 26, wherein the
contacts each are provided with a diameter of about 10 μm .

1 41. The method according to claim 26, wherein the
2 contacts each are provided with a diameter of less than
about 10 μm .

1 42. The method according to claim 26, wherein the
2 contacts are provided with a pitch of less than about 100
 μm .

1 43. The method according to claim 26, wherein the
contacts are provided with a pitch of about 30 μm .

1 44. The method according to claim 26, wherein the
2 contacts are provided with a diameter about 20 % of the
diameter of the first solder bumps.

1 45. The method according to claim 26, wherein the
2 contacts are provided with a smaller size than the first

solder bumps.

1 46. The method according to claim 26, wherein the
2 contacts provide optical communication between the first
substrate and the second substrate.

1 47. The method according to claim 26, wherein the
contacts comprise a waveguide.

1 48. The method according to claim 26, wherein the
2 contacts comprise an optical transmitter and an optical
receiver.

1 49. The method according to claim 26, wherein the
2 contacts comprise at least one member selected from the
3 group consisting of dendrites and self-interlocking micro
connectors.

1 50. The method according to claim 26, wherein the
2 contacts and the first solder bumps are provided such that
3 an upper surface of the contacts and an upper surface of the
first solder bumps are co-planar.

1 51. The method according to claim 26, wherein the

